University of California, Santa Cruz
Electrical and Computer Engineering Department
ECE-171, Summer 2022

Analog Electronics

ECE171 Lecture Room: J Bask Aud 101. MW 8:00 – 9:40 AM
ECE171/L Laboratory Room: J Bask, Rm 161
Instructor: Jeorge S. Hurtarte (jhurtart@ucsc.edu)
Office: via Zoom by Appointment

Course Description:

This course introduces basic passive and active analog devices required for the analysis and engineering design of modern discrete electrical circuits, both analog and digital. Students are expected to possess a working knowledge of basic electrical engineering network analysis techniques; (ECE101 or equiv.), linear systems theory (ECE103 or equiv.) are recommended. Understanding linear systems is important for this class; relevant topics will be introduced and discussed as needed.

Note: In order to take the Lab, ECE171/L, you must be concurrently enrolled in ECE 171 or have taken it previously.

General coverage will include the following topics (but not necessarily in the order shown):

- Basic system theory, signals, linearity and distortion, time and frequency domain perspectives and analysis.
- The operational amplifier; ideal and non-ideal op-amp characteristics. How to use the op-amp in engineering design.
- Junction devices including diodes, bipolar junction transistors (BJT) and field-effect transistors (FET): relevant solid-state physics, basic biasing techniques, large and small-signal analysis and design, amplifier (BJT and FET) and switching characteristics, *h-parameters*, basic open-loop analog circuit configurations. We will survey fundamental field-effect types, JFET and MOSFET; enhancement and depletion modes; NMOS, PMOS and CMOS digital circuits.
- Differences between the design of discrete and integrated circuits.
- Introduction to PSPICE or equivalent.

References:
Required: Microelectronic Circuit Design, Jaeger, Blalock and Blalock, McGraw-Hill 2022, 6th ed.
Useful: Microelectronic Circuits, Sedra and Smith, Oxford 2015, 7th ed.

Optional Lab text: Pspice for Basic Microelectronics, Tront, McGraw-Hill Higher Education 1st ed. 2008.

Supplementary references will be discussed in lecture. Many of these will be industrial application notes, typically in PDF format and will be made available on our website.

Lecture Notes are available as a printed reader. All of them will posted to our Canvas website for ready access. Interested students can obtain printed copies by ordering them from UCSC Professor Publishing located in the Baskin Engineering Building.

Homework:

Homework will be assigned and collected in Canvas and will generally follow a weekly sequence. Material will consist of problems from our text. To receive full credit, your work must be well organized, written at a college level and show evidence of thoughtful attention to the problem itself.

Examinations: There will be one midterm exam and a comprehensive final exam.

Grading will be based on college level writing, completeness, clarity, and conceptual understanding. The rubric is as follows:

> **Exposition:**
> Was the writing relevant, organized, clear and at college level? Did it support the conceptual and mathematical topics discussed? Note: first draft quality writing will receive no exposition credit.
>
> **Conceptual Understanding:**
> Were relevant concepts understood?
>
> **Mathematical Completeness:**
> Was relevant math expressed and used correctly, reinforcing and justifying relevant concepts? Was it adequately introduced and explained? Were analytic results or statements justified?

Unless otherwise stated, Conceptual = 40%; Math = 40% and Exposition=20%. A uniformly distributed mapping will be employed to equate percentages to letter grades:

A+ >= 100; A >= 85; A- >=80; B+ >=75; B >=60; B- >=55; C+ >=50; C >=35; C- >=30; D+ >=25; D >=10; D- >= 5: F >=0

Grading: Letter grades will be assigned for all work. Averaging will follow the usual 4.0 point scale to determine a final grade-point and associated letter grade. Category weightings are as follows:

Homework	33%	
Midterm Exam	33%	
Final Exam	34%	passing this test is required to pass the class.

Academic Integrity:
The student-instructor relationship is based on imputed trust. Violations of this trust by deceptively offering the work of others as your own, cheating on examinations etc. will result in formal charges of academic dishonesty being brought against you.

DRC accommodation requests should be received by the first week of class.